PLEASE AMEND THE CLAIMS AS FOLLOWS:

Claim 1. (currently amended) A method of forming a strained semiconductor layer, comprising the steps of:

providing a first wafer with a surface comprising of a first semiconductor layer of a first natural lattice constant;

forming a second semiconductor layer with a second natural lattice constant on the first semiconductor layer, with a strain gradient introduced at the interface of said second semiconductor layer and said first semiconductor layer;

providing a second wafer with a surface with or without an insulator layer;

bonding said second semiconductor layer on said surface of said second wafer, resulting in a third wafer comprised of said second wafer, said second semiconductor layer, and said first wafer; and

performing a water jet cleaving procedure at said strain gradient so that said second semiconductor layer is separated from said first semiconductor layer and said first wafer.

Claim 2. (original) The method of claim 1, wherein said second wafer is a single crystalline silicon substrate.

Claim 3. (original) The method of claim 1, wherein said second wafer is a single crystalline silicon substrate with an overlying insulator layer formed on it.

Claim 4. (original) The method of claim 3, wherein said insulator layer is a silicon dioxide layer.

Claim 5. (original) The method of claim 3, wherein said insulator layer is a silicon nitride layer.

Claim 6. (original) The method of claim 1, wherein said first semiconductor layer has a lattice constant greater than that of overlying said second semiconductor layer.

Claim 7. (original) The method of claim 1, wherein said first semiconductor layer is an alloy semiconductor layer comprising silicon and germanium.

Claim 8. (original) The method of claim 1, wherein said first semiconductor layer is an alloy semiconductor layer comprising of silicon and germanium, epitaxially grown to a thickness between about 0.1 to 10 microns, with a Ge mole fraction between about 5 to 80%.

Claim 9. (original) The method of claim 1, wherein said second semiconductor alloy layer is a silicon layer under tensile strain.

Claim 10. (original) The method of claim 1, wherein said second semiconductor layer is a silicon layer, epitaxially grown to a thickness between about 20 to 1000 Angstroms.

Claim 11. (currently amended) A method of fabricating a metal oxide semiconductor field effect transistor (MOSFET) device on an insulator layer, featuring a silicon channel region, comprising the steps of:

providing a first wafer with a surface comprising of a first semiconductor material of a first natural lattice constant;

forming a second semiconductor layer with a second natural lattice constant on the first semiconductor material so that said second semiconductor layer is strained, and with a large strain gradient formed at the interface of said second semiconductor layer and said first semiconductor material;

providing a second wafer comprising of a substrate with an overlying insulator layer;

bonding said second semiconductor layer on said second wafer, with an insulator in between, resulting in a third wafer comprised of said second wafer, said second semiconductor layer, and said first wafer;

performing a compressed air or pressurized fluid cleaving procedure at said strain gradient so that said second semiconductor layer is separated from said first semiconductor material, resulting in a fourth wafer comprised of said second semiconductor layer and said second wafer; and

forming a MOSFET device on said fourth wafer, comprising of a gate structure and of source and drain regions located adjacent to said gate structure.

Claim 12. (original) The method of claim 11, wherein said second wafer is a silicon wafer with an insulator formed on it.

Claim 13. (original) The method of claim 12, wherein said insulator layer is a silicon dioxide layer.

Claim 14. (original) The method of claim 12, wherein said insulator layer is a silicon nitride layer.

Claim 15. (original) The method of claim 11, wherein said first semiconductor material is an alloy semiconductor layer comprising of silicon and germanium in a relaxed state.

Claim 16. (original) The method of claim 15, wherein said alloy semiconductor layer is obtained by epitaxial growth procedures.

Claim 17. (original) The method of claim 15, wherein said alloy semiconductor layer is epitaxially grown to a thickness between about 0.1 to 10 microns, with a Ge mole fraction between about 5 to 80%.

Claim 18. (original) The method of claim 11, wherein said second semiconductor layer is a silicon layer.

Claim 19. (original) The method of claim 18, wherein said silicon layer is epitaxially grown to a thickness between about 20 to 1000 Angstroms.

Claims 20 - 27 (cancelled)